World Class Verilog & SystemVerilog Training

Sunburst Design - Expert Verilog-2001 FSM, Multi-Clock Design & Verification Techniques

by Recognized Verilog & SystemVerilog Guru, Cliff Cummings of Sunburst Design, Inc.

Cliff Cummings is the only Verilog & SystemVerilog Trainer who helped develop every IEEE & Accellera Verilog, Verilog Synthesis and SystemVerilog Standard.

2 Days
60% Lecture, 40% Lab
Advanced Level

Course Objective

Simply stated, to give engineers *world class* Verilog, synthesis & verification training using award winning materials developed by renowned Verilog & SystemVerilog Guru, Cliff Cummings

Upon completion of this course, students will:

- Write efficient synthesizable Verilog-2001 RTL models
  - includes six different FSM coding styles
  - includes multi-clock and FIFO design techniques
  - includes experimentation with different synthesis coding styles
- Write complex self-checking testbenches
  - includes working with actual Verilog project directory structures in all labs
  - includes using proven techniques for generating self-checking tests

Course Overview

Sunburst Design - Expert Verilog-2001 FSM, Multi-Clock Design & Verification Techniques is a 2-day fast-paced advanced topics and expert design techniques course with instruction on Verilog self-checking testbench creation. This is a design course, not a language syntax course.

The 500+ page binder for this 2-day course covers expert Verilog-2001 design techniques. Numerous proven RTL coding guidelines are taught and explained.

Complete coverage of blocking and nonblocking assignments is presented using materials from two of Cliff's award-winning presentations on nonblocking assignments. 70 slides and a copy of an award-winning paper on nonblocking assignments with delays support the coding guidelines presented. Additional materials show transport delay-mode modeling for mixed RTL and gate-

level simulation. 100+ pages will help you to master one of the most difficult and powerful topics in the Verilog language. No other course comes close to this coverage.

Another 100+ slides and two more award winning papers help to demonstrate multiple Finite State Machine (FSM) expert techniques including detailed techniques using four efficient FSM coding styles, and warnings about two common and inefficient coding styles. Labs include PCI bus arbiters and partial PCI target FSM designs (no silly traffic-light controllers, black jack games or soda pop change machines in this course!)

Included in the class are techniques for doing multi-asynchronous clock design. These techniques are not only advanced Verilog techniques, they are also advanced digital design techniques not covered by college courses. With more than 100 slides dedicated to this section and three award-winning and highly acclaimed papers for added reference material, this section alone is worth the price of admission.

Engineers will be shown the tricks and techniques used to build all of the self-checking testbenches used to test the RTL models developed in this course and other Sunburst Design training courses. Verification techniques will be shared for creating self-checking testbenches, including correct application of stimulus vectors and proper timing of output capture for verification while making use of the "SIMUTIL" self-checking testbench tasks and functions that were used to write all of the testbenches for the synthesis labs. All students will be given a copy of the SIMUTIL testbench utilities to take back and use at their own companies on their own designs.

A 500+-page student guide and 49-page Verilog-2001 HDL Quick Reference Guide supplement the lecture and provide excellent reference material for after the class. Numerous exercises and labs reinforce the principles presented. After you take this course, you will understand why Cliff Cummings has won 13 "Best Paper" awards for presentations made over the past 13 years.

Target Audience

Sunburst Design - Expert Verilog-2001 FSM, Multi-Clock Design & Verification Techniques

Target Audience

Sunburst Design - Expert Verilog-2001 Design, RTL Synthesis & Verification Techniques is intended for the most experienced ASIC and FPGA design and verification engineers that require in-depth instruction on expert Verilog-2001 RTL synthesis state machine design techniques, advanced multi-clock design techniques, advanced FIFO design techniques and Verilog verification skills.

Prerequisites (mandatory)

This is a design course, not a language syntax course. This course assumes that students have a practical working knowledge of Verilog HDL or have completed Verilog HDL training. Engineers with VHDL synthesis experience and some Verilog exposure will do well in this class. Engineers with no prior HDL training or experience will struggle in this class. *This is an advanced class, not just an advanced beginner class!*

The Sunburst Design - Advantage

Who is teaching your "expert" and "advanced" classes? Most companies will not tell you because their instructors might not have much design experience or may never have participated on any of the Verilog Standards groups or presented at industry recognized conferences. Go to our web site and read about the Sunburst Design - Instructors - they are simply the best at what they do and they have the experience and qualifications to offer best-in-class training.

Sunburst Design Courses:

- *Sunburst Design - Advanced SystemVerilog for Design & Verification* - 4 days
  - *Sunburst Design - Advanced SystemVerilog for Design* - 3 days
  - *Sunburst Design - Advanced SystemVerilog for Verification* - 3 days
- *Sunburst Design - Expert Verilog-2001 for Synthesis & Verification* - 4 days
  - *Sunburst Design - Expert Verilog-2001 RTL Synthesis Coding* - 2 days
  - *Sunburst Design - Expert Verilog-2001 FSM, Multi-Clock Design & Verification Techniques* - 2 days
- *Sunburst Design - Comprehensive Verilog-2001 Design & Best Coding Practices* - 4 days
  - *Sunburst Design - Introduction to Verilog-2001 & Best Coding Practices* - 2 days
  - *Sunburst Design - Advanced Verilog-2001 Knowledge & Design Practices* - 2 days
  - *Sunburst Design - Accelerated Introduction to Verilog-2001 & Best Known Coding Practices* - 1 day
- *Advanced Verilog PLI Courses* - (taught by a Sunburst Design training partner)

Course Customization? - Sunburst Design courses can be customized to include ***your*** company's coding guidelines or to modify the course for a different audience. Sections can be added or deleted from a course to meet you company's needs.

Course Syllabus

Day One

Nonblocking Assignments
- Detailed instruction on how Verilog blocking and nonblocking assignments work. Verilog scheduling algorithms are discussed and blocking and nonblocking assignment synthesizable model, usage-guidelines are presented. Includes important information that must be considered when doing mixed RTL and gate-level simulations.

- Simple flip-flops
- Blocking assignments
- Nonblocking assignments
- Inertial and transport delays
- Delay lines
- Mixed RTL & gate-level simulations
- Guidelines

IEEE Verilog 2001 Enhancements
- A concise summary of the important IEEE Verilog-2001 enhancements for both design and verification.

- The V2K1 top-5 enhancement requests
- V2K1 Multi-dimensional arrays
- Array of Instances (AOI) & V2K1 generate statements
- V2K1 Enhanced File I/O
- V2K1 reentrant tasks and functions
- V2K1 configurations
- New V2K1 port and parameter styles
- V2K1 sensitivity lists
- V2K1 RTL enhancements
- V2K1 signed arithmetic
- V2K1 IP development enhancements
- V2K1 miscellaneous enhancements
- Guidelines
- Labs: Combinational labs II

State Machines
- Fundamental and advanced coding styles for state machines. Includes important considerations for coding designs for easy debug and optimal synthesis. Why parameter state definitions are used instead of `define. Binary encoded, and efficient onehot coding styles are presented. FSMs with combinational outputs and sequential outputs are also presented.

- State machines
- Moore & Mealy styles
- Two always blocks implementation - combinational outputs
- Output assignments using always blocks and continuous assignments
- One always block implementation - Inefficient - avoid this style
- Three always block coding style - registered outputs
- Indexed one-hot implementation - registered outputs
- Encoded one-hot implementation - Inefficient - avoid this style
- Output encoded style - registered outputs
- Modified Mealy FSM to register outputs
- Efficiencies
- An early look at SystemVerilog 3.0 enumerated types
- Quick introduction to multi-clock design issues
- Labs: State machine labs experimenting with different coding styles and the "full_case parallel_case" synthesis directives. Simple multi-clock FIFO lab (behavioral model)

Day Two

Multi-Clock Design
- Detailed material for efficient coding, synthesizing, and verifying of multi-clock designs, taken from actual design experiences.

- Multi-clock metastability and synchronization
- Multi-bit synchronization
- Multi-clock design techniques
- Multi-clock partitioning and naming conventions
- Synthesis scripting considerations
- Static timing analysis considerations
- Gate-level simulation considerations

Multi-Clock FIFO Design
- Detailed material for efficient implementation of multi-clock FIFO designs.

- Multi-clock FIFO simulation inadequacies
- Gray codes
- RTL Gray code counters (ASIC vs. FPGA tradeoffs)
- Synchronized RTL FIFO coding style
- Asynchronous full-empty FIFO coding style technique

Testing & Testbenches
- This section covers various testbench stimulus and verification techniques, including use of Verilog tasks to generate bus functional models. Includes a detailed discussion of hierarchical referencing to probe designs and generate self-checking testbenches. Also details the contents of SIMUTIL, a set of simulation tasks for rapid development of self-checking testbenches.

- V2K1 named parameter passing and defparam avoidance
- V2K1 file I/O enhancements
- An early look at .name and .* SystemVerilog 3.0 implicit port connections
- Testing approaches
- Advanced loops, tasks, and functions & V2K1 automatic tasks and functions
- Bus functional model testing
- Global variables
- Hierarchical referencing
- ASCII "string" display
- Another early look at SystemVerilog 3.0 enumerated types
- Dumpfiles and waveform viewer strategies
- Self-checking tests
- Correct timing and techniques for applying stimulus and verifying results
- SIMUTIL self-checking testbench tasks
- Regression test generation
- Self-adapting pipeline testing

Classroom Details
Training is generally conducted at your facilities. For maximum effectiveness, we recommend having one workstation or PC for every two students, with licenses for your preferred Verilog simulator (we often can help provide the simulator and temporary training licenses).

For more information, contact:

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