
**World Class SystemVerilog & UVM Training**

# ***Sunburst Design - Expert Clock Domain Crossing (CDC) & FIFO Design Techniques using SystemVerilog***

by Recognized Verilog & SystemVerilog Guru, Cliff Cummings of Sunburst Design, Inc.

*Cliff Cummings is the only Verilog & SystemVerilog Trainer who helped develop every IEEE & Accellera Verilog, Verilog Synthesis and SystemVerilog Standard.*

**1 Day**
**60% Lecture, 40% Lab**
**Expert Level**

## Course Syllabus - 1-day Course

**Multi-clock Clock Domain Crossing (CDC) & FIFO Design Techniques using SystemVerilog**
- Very advanced design techniques from Cliff's award-winning presentations on the efficient implementation of multi-clock CDC & FIFO designs. These materials are not specific to SystemVerilog but solutions are shown using SystemVerilog syntax (advanced techniques that all design engineers should know - the stuff you did not learn in college).

- (1) Metastability & synchronizers - synchronizing 1-bit signals
- (2) Passing multiple control signals - synchronizing multi-bit signals or busses
    a. Consolidation
    b. Controlled synchronization - multicycle path formulations (MCP)
    c. FIFO synchronizer
    d. Gray codes & Gray code counters
- (3) Design partitioning - design & synthesis techniques
    a. Naming conventions
    b. Synthesis scripting & timing analysis issues
- (4) Simulation issues
    a. X-propagation issues
    b. Synopsys command for SDF files
    c. Multi-SDF files
    d. ASIC/FPGA vendor cells and models
    e. Simulation model to expose synchronization problems
- (5) Multi-clock FIFO design - large section on design and FIFO issues
- LAB: MCP controlled synchronization lab
- LAB: 2-clock FIFO lab